2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)

High Stability Adaptive LDO using Dynamic Load Sensing for Low Power Management of Wireless Sensor Networks

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2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES) | 978-1-7281-5672-9/20/$31.00 ©2020 IEEE | DOI: 10.1109/PEDES49360.2020.9379765

Abstract—**Presented in this paper is the design of a low-dropout voltage regulator implemented in 65nm CMOS technology for low power management of wireless sensor networks for IoT technology. High stability is achieved using a dynamic load sensing technique where the sensed load current adjusts the bias of the error amplifier. The dynamic mechanism provides low/high bias current to the error amplifier as the load current decreases/increases, respectively. The LDO adapts and transforms from a 2-stage configuration at light-loads to a 3-stage configuration at high-load conditions for a more current-efficient system. Two power transistors are activated depending on the load conditions, with the main power transistor activated only if the load current is greater than the threshold current I_{on} of 919.11µA, allowing for wide range of load application from 0 to 100 mA. Simulation results confirm that adaptive biasing technique through dynamic load sensing and subthreshold operation of the system enables the LDO to achieve ultra-low quiescent current of 930.21nA with power consumption of 744.17nW at no-load. A regulated output voltage of 600mV from 800mV to 1.2V supply voltage with a dropout voltage of 135mV.**

Keywords—ultra-low quiescent current LDO, adaptively-biased LDO, adaptive biasing, dynamic load sensing

I. INTRODUCTION

Power management system is developed employing efficient and reliable voltage regulators to meet the demands of silicon area scaling and low power consumption. In applications where low power consumption is required, efficient voltage regulation techniques using low-dropout (LDO) regulator aims to supply a stable and constant voltage despite battery, ambient, and load conditions [1-2]. Advantages include increase in battery life and ripple rejection in supply voltage in wireless sensor networks (WSN) circuits by providing a regulated and accurate supply voltage for noise-sensitive analog blocks.

An off-chip capacitor usually in µF range is used to achieve stable operation but, a trade-off on silicon area and power consumption. Modern designs imply accuracy, power efficiency, and improved response times, less silicon area and less off-chip components (capacitor). This motivates design innovations of embedded output-capacitorless LDO in system-on-chip applications. However, the recent trend in output-capacitorless LDO pose greater design challenges in system stability and load transient response. In low power design restrictions, output impedance in gain stages is high, causing poles to locate at low frequencies [3]. An underlying issue in low voltage transistors is reduced gate drive for power transistor implying lesser output current capability.

In this study, an ultra-low power output-capacitorless LDO voltage regulator is designed to maintain steady operation and stability under varying load conditions with low quiescent current to significantly reduce power consumption even at the inactive state or sleep mode of the wireless sensor nodes. In order to gain stability and enhanced transient performance under ultra-low power design constraints, a technique using adaptive power transistors which allows the regulator to transform between two- and three- multi gain stages as load current varies from 0mA to 100mA. This offers ultra-low quiescent current at no-load condition, system stability across the whole load range of 0mA to 100mA, and high current efficiency.

A. Conventional Low-dropout Voltage Regulator

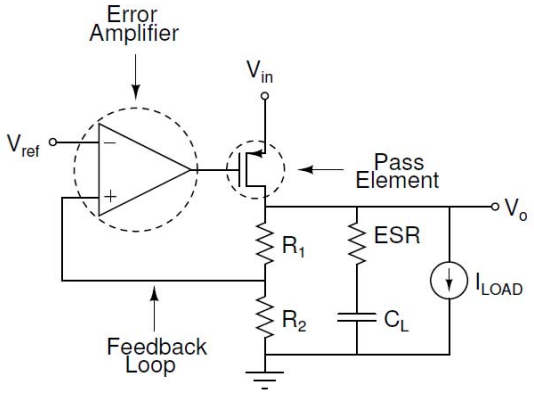

Figure 1. Conventional LDO voltage regulator schematic [4].

Main blocks of the conventional LDO topology are the error amplifier, pass device and linear feedback network (R_1 and R_2) as shown in Fig. 1. An error amplifier compares the difference between the reference voltage and the output voltage obtained by the resistive feedback network. A pass device controls the amount of current flow to the load. This device is typically large, as it needs to drive the total load current. Finally, a large capacitor at the LDO output is placed parallel to the load which sets the dominant pole and LHP zero, thereby improving the stability of the circuit and good power supply rejection. Its large capacitance value also serves as a charge/discharge outlet during sudden load current changes to improve the system's transient response.

Fig. 2 depicts comparison between a conventional off-chip LDO and the output-capacitorless LDO. With the latter topology, absence of external load capacitance results to reduction of PCB area and external pins, and pad and package

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connections, making it very suitable for system-on-chip (SoC) designs such as WSN applications.

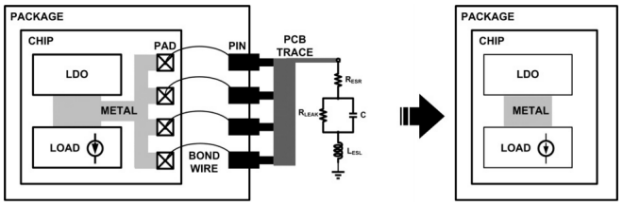


Figure 2. Conventional off-chip LDO vs. Capless LDO [4].

B. System stability of conventional LDO

Fig. 3 is the abstraction model of conventional LDO where system transfer function is derived.

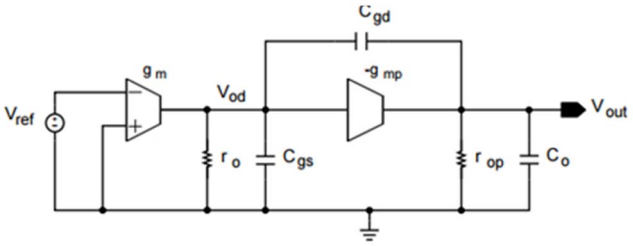


Figure 3. Conventional LDO abstraction model [4].

System stability requires that the zero must be below UGF and all high-frequency poles at frequencies higher than UGF. The zero and poles are given by equations 1 to 3:

$$Z = \frac{gmp}{Cgd} \tag{1}$$

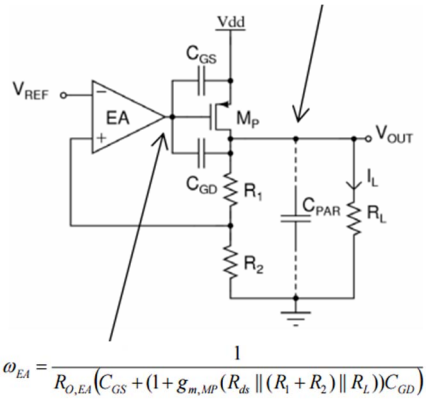
$$P1 \cong -\frac{1}{(Co+Cgd)rop+(Cgs+Cgd)ro+Cgd*ro*rop*gmp} \tag{2}$$

$$P2 \cong -\frac{gmp}{Co\,(Cgs+Cgd)} \tag{3}$$

The large capacitor sets the dominant pole at the output of the LDO. This compensates the high output impedance of the LDO, for a more reliable instantaneous source of current improving the LDO transient response. The non-dominant pole is defined by the pass device characteristics, and the zero is defined by the transconductance and gate drain capacitance.

C. Multi-gain stages output-capacitorless LDO

$$\omega_{OUT} = \frac{1}{C_{PAR}(R_{ds} \parallel (R_1+R_2) \parallel R_L)}$$



$$\omega_{EA} = \frac{1}{R_{O,EA}\left(C_{GS}+(1+g_{m,MP}(R_{ds} \parallel (R_1+R_2) \parallel R_L))C_{GD}\right)}$$

Figure 4. Two-gain stage LDO structure [4].

In a two-gain stage output-capacitorless LDO as illustrated in Fig. 4, the dominant pole is set at the error amplifier. For stability, output pole has to be located within unity gain frequency (UGF). The equations show that poles are a function of load current.

$$\omega_{EA} \propto \sqrt{I_L} \;\; ; \;\; \omega_{OUT} \propto I_L \;\; ; \;\; \omega_{OUT} >> \omega_{EA} \tag{4}$$

In Fig. 5, output pole ω_{OUT} moves closer to the dominant pole ω_{EA} as load current is reduced. This reduces the phase margin at light load conditions, affecting its stability at light loads.

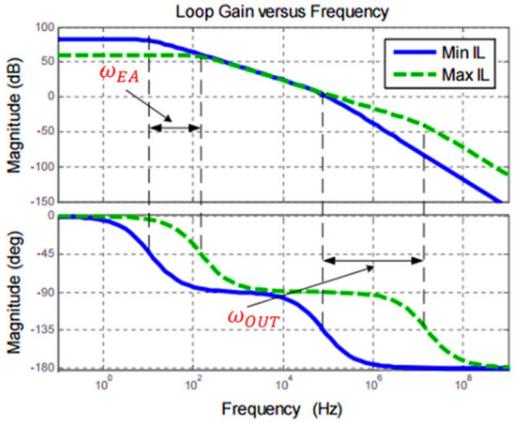


Figure 5. 2-gain stage LDO stability and pole movement [4].

A three-gain stage structure in Fig. 6 is a cascade of first-order and second-order filters. Dominant pole is set by the integrator and non-dominant poles by the biquad. As shown in Fig. 7, complex non-dominant poles are formed with peaking effect. This instability happens at light load conditions.

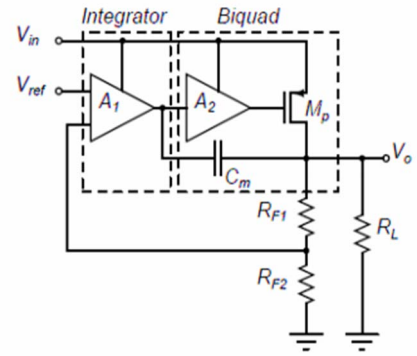


Figure 6. Three-gain stage LDO structure [4].

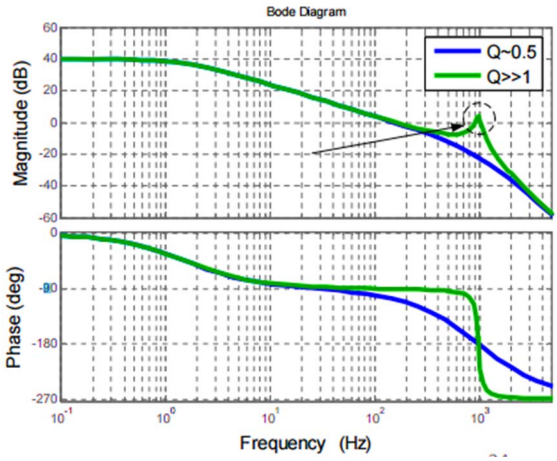


Figure 7. 3-gain stage LDO stability and pole movement [4].

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II. SYSTEM DESIGN AND ARCHITECTURE

A. Proposed topology of LDO Voltage Regulator

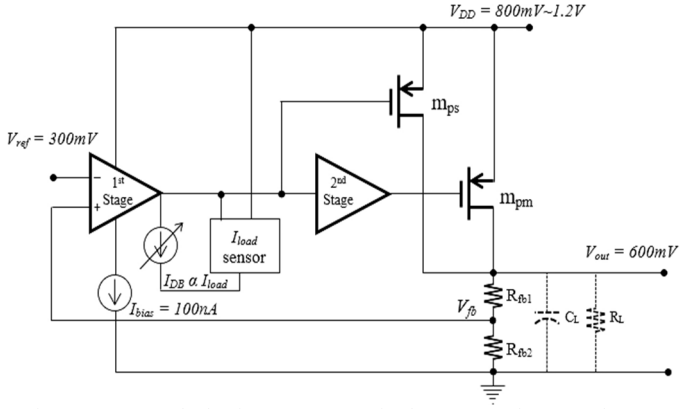

Figure 8. Proposed adaptive output-capacitorless LDO voltage regulator with dynamic load sensing.

The proposed architecture in Fig. 8 is an adaptively biased LDO voltage regulator which comprises a 1st gain stage error amplifier, 2nd gain stage non-inverting amplifier, a sub-power transistor M_{ps}, main power transistor M_{pm}, and feedback network composed of R_{fb1} and R_{fb2} [4]. Output current is delivered via the power transistors where the gate voltages are controlled by the error amplifier [4]. An off-chip parasitic capacitance C_L is due to on-chip power distribution and load parasitic simulated at 50pF to 100pF.

The error amplifier is biased by a constant bias current (I_{bias}) at 100nA and the dynamic current (I_{db}) from the load current sensor which enables low-voltage and high precision regulation [5-6]. The I_{load} sensor gives larger bias current (I_{db} = δ x I_{load}) to the error amplifier at heavy load. With adaptive biasing technique, the dynamic bias current I_{db} is large at load currents greater than 1mA, and during load transition from heavy to light load, large initial gate charging current of the pass device reduces V_{gs} quickly to reduce overshoot. At light load condition less than the defined threshold current I_{on} of 919.11µA, transistor M_{pm} is turned off and the dynamic load current sensor provides low bias current proportional to the current of transistor M_{ps}. Thus, achieving ultra-low quiescent current and improve current efficiency at light loads. When the load current exceeds I_{on}, transistor M_{pm} is turned on and the biasing current I_{db} stops and becomes stable/fixed. The proposed regulator is then transformed into a 3-gain stage structure. The bias current of the error amplifier increases as load current increases from light to heavy load and pushes the poles in higher frequencies, thus, increasing bandwidth.

B. System Stability

Cascode frequency compensation is used in this topology for high current efficiency, higher bandwidth and enhanced power supply rejection. Stability margins and locations of the poles and zeroes of the two structures are defined per gain structure. For the 2-stage structure, $I_{load}<I_{on}$, the 2nd gain stage non-inverting amplifier is operating in linear region and transistor M_{pm}, is turned off. Fig. 9 is the small-signal model where R_o is the effective output resistance with R_{omps} as the sub-power transistor resistance, R_{fb} as the feedback resistance and R_{load} as load resistance.

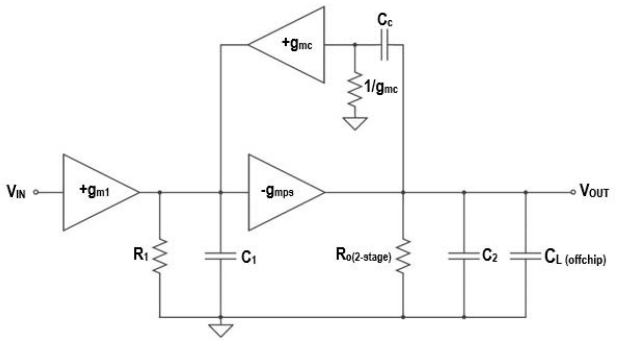

Figure 9. Small-signal of 2-gain stage LDO structure.

Stability margins, poles and zeroes are defined by:

Effective output resistance: $Ro = Ro_{mps}||R_{fb}||R_{load}$ (5)

DC gain : $A_{dc} = g_{m1}g_{mps}R_1R_{o(2-stage)}$ (6)

Dominant pole : $P_{-3dB} = -\frac{1}{Cc\ g_{mps}\ R1\ Ro}$ (7)

Pole 2 : $P_2 = -\frac{Cc\ g_{mps}}{C1\ CL}$ (8)

Pole 3 and zero : $P_3 = Z = -\frac{gmc}{Cc}$ (9)

For the 3-stage structure, $I_{load} > I_{on}$,the 2nd gain stage non-inverting amplifier and transistor M_{pm}, are already activated and included in the analysis. Fig. 10 shows the small-signal model of the 3-stage structure where R_o is the effective output resistance with R_{omps} as the sub-power transistor resistance, R_{ompm} as the main-power transistor resistance, R_{fb} as the feedback resistance and R_{load} as load resistance.

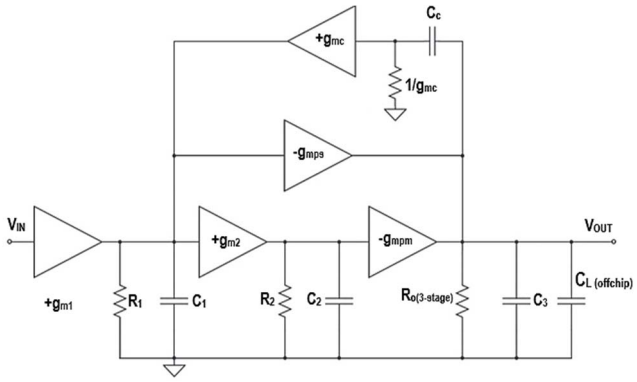

Figure 10. Small-signal of 3-gain stage LDO structure.

Stability margins, poles and zeroes are defined by:

Effective output resistance:

$Ro = Ro_{mps}||Ro_{mpm}||R_{fb}||R_{load}$ (10)

DC gain : $A_{dc} = g_{m1}g_{m2}g_{mpm}R_1R_2R_o$ (11)

Dominant pole : $P_{-3dB} = -\frac{1}{Cc\ g_{m2}g_{mpm}R_1R_2R_o}$ (12)

Non-dominant poles 2,3 : $|P_{2,3}| = \sqrt{\frac{g_{m2}g_{mc}g_{mpm}R_o}{C_1C_2}}$ (13)

Non-dominant pole 4 : $P_4 = -\frac{1}{C_LR_o}$ (14)

Zero 1 : $Z_1 = -\frac{g_{mc}}{C_c}$ (15)

Zero 2 : $Z_2 = -\frac{g_{m2}g_{mpm}}{C_2g_{mps}}$ (16)

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The dominant pole is the only pole within UGF and located at the output of the error amplifier. Loop stability now depends on P_2 location and is pushed to higher frequencies due to cascode compensation. Therefore, stability is worse at no-load of 0mA. Phase margin and system stability improves as load current is increased with the aid of increased bias current of the error amplifier thru dynamic biasing, since poles are pushed to higher frequencies.

C. Design and Implementation

The proposed adaptive output-capacitorless low-dropout voltage regulator has target specifications in Table 1.

TABLE 1 Target Design Specifications

Specification	Value
Input Voltage Range - V_{DD}	0.8V – 1.2V
Output Voltage	600 mV
Dropout Voltage	< 200 mV
Load Current	1pA ~ 100 mA
Quiescent Current	< 1µA
Power Dissipation	< 5 µW
Technology	65nm CMOS

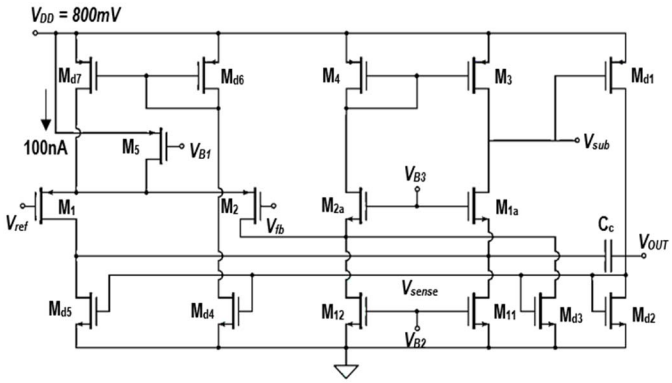

Figure 11. Schematic of dynamically-biased error amplifier

The dynamically-biased error amplifier in Fig. 11 is composed of M_5 which is biased at 100nA tail current from the bias generator with mirrored transistors M_3 and M_4 which converts differential signal into a single output signal in the drain current of M_{2a} to the output. The dynamic current sensor comprised of transistors M_{d1}-M_{d7} with M_{d2}-M_{d4} mirrored to have the same gate, drain and source voltages, better sensing of load current and improved bandwidth on moderate load conditions.

The DC gain of the circuit is given by:

$$Av = g_m R_o \quad (17)$$

where g_m is the transconductance and R_o is the output resistance. Because of the current mirror of transistors M_{1a} and M_{2a}, and M_3 and M_4, the transconductance is mainly contributed by the variation in the drain-current M_1 and M_2;

$$g_m = g_{m1} = g_{m2} \quad (18)$$

$$R_o = (R_{out}|M_3)||(R_{out}|M_{1a}) \quad (19)$$

The power transistors M_{ps} and M_{pm} are the sub and main power transistors, respectively. The regulator works in subthreshold region in steady state, except the power transistors in saturation. Low-voltage operation is allowed with lower quiescent current. Larger transistor sizes in W/L are needed to maintain subthreshold operation and good matching. The current of the transistors in subthreshold is given by:

$$Id_{sub-vth} = I_{so}\frac{W}{L}e^{\frac{V_{gs}}{nV_T}}\left(1 - e^{\frac{-V_{ds}}{V_T}}\right)(1 + \lambda_{sub}V_{ds}) \quad (20)$$

The drain current of the transistors in saturation is given by:

$$Id_{saturation} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})(1 + \lambda_{sat}V_{ds}) \quad (21)$$

In the 2-stage structure, the sub-power transistor, M_{ps}, supplies the load current. M_{d1} copies current from M_{ps} and a gate voltage, V_{sense}, which varies with the obtained load current. As the load increases, the dynamic load current sensor also increases bias current of the error amplifier. As load current increases beyond I_{ON}, current in the sub-power transistor M_{ps} becomes stable and the extra current is supplied by the main power transistor, M_{pm}. Simulated threshold current I_{ON} is 919.11µA. In the 3-stage structure, the non-inverting amplifier acts as the 2nd gain stage and transistor M_{pm} *is* the 3rd gain stage. The sub-power transistor M_{ps}, and M_c are driven by the dynamically biased 1st gain stage. The two transistors are mirrored with current ratio 1: M. When I_{LOAD} is low, current $I_{n3} = I_{load}/M$ (a factor of the load current). M_{p2} is biased to source a current of $I_d = NxI_b$. When $I_{n3} < I_d$, transistor M_{p2} operates in triode region, the node V_{main} is pulled up close to V_{DD} turning transistor M_{pm} off. Pole at V_{main} is at higher frequencies despite gate parasitics at M_{pm}. When I_{LOAD} increases at the transition bias point where $I_{N3} \geq I_d$, transistor M_{pm} starts to operate in saturation region.

III. RESULTS AND DISCUSSION

The proposed output-capacitor-free adaptive LDO voltage regulator is designed and implemented 65nm CMOS technology. For a supply voltage of 800mV$_{DD}$ and ideal reference voltage of 300mV, the regulator is capable of supplying load current from 1pA~100mA with a regulated output voltage of 600mV and a dropout voltage of 135mV. Compensation capacitor, Cc of 3.5pF stabilizes the system from no-load to full-load. An off-chip capacitor of 50pF and 100pF is used to model the load parasitics C_L. At no load, quiescent current of the integrated system has a total quiescent current of 930.21nA.

Fig. 12 shows the stability margins – open-loop gain and phase margin with C_L=50pF at different load currents 1pA to 100mA. Results in Table 2 show that system is stable for the entire load range of 0mA to 100mA. Worst condition happens at no-load condition since the gate discharging current of the error amplifier is quite small to source current to the load. Stability becomes better as load increases.

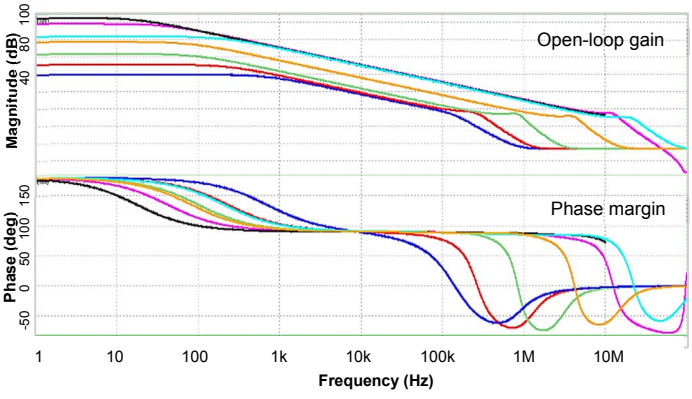

Figure 12. Frequency response for I_{LOAD} = 1pAto 100mA

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TABLE 2 Open-loop gain and phase margin measurements

Parameter	1pA	1µA	100µA	1mA	10mA	100mA
Gain	40dB	51.3dB	77.5dB	83.7dB	105.5dB	98.4dB
PM	49.6°	77°	90.2°	89.7°	88.4°	82.4°

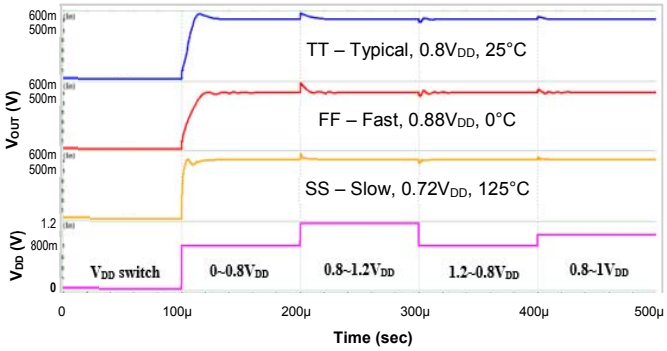

Figure 13. Plot on transient line regulation at Δt=100ps

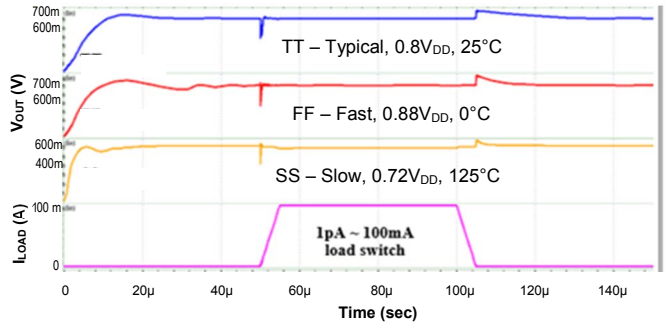

Figure 14. Plot on transient load regulation

The transient response of the system is simulated at different corners (TT, FF, SS), that is at varying processes (typical, fast, and slow), voltage, and temperature conditions. The transient line regulation is in Fig. 13 illustrates that the worst condition occurs at 0.8 to 1.2 V_{DD} switch at ff process corner, with 93mV overshoot which settles at 11µs and ripple voltage of 0.53%. The transient load regulation at 1pA to 100mA load switch with Δt=3µs is in Fig. 14. Worst condition happens at ff process corner having 90.3mV overshoot and 119mV undershoot which settles at 27.9µ and low ripple of 0.00125%.

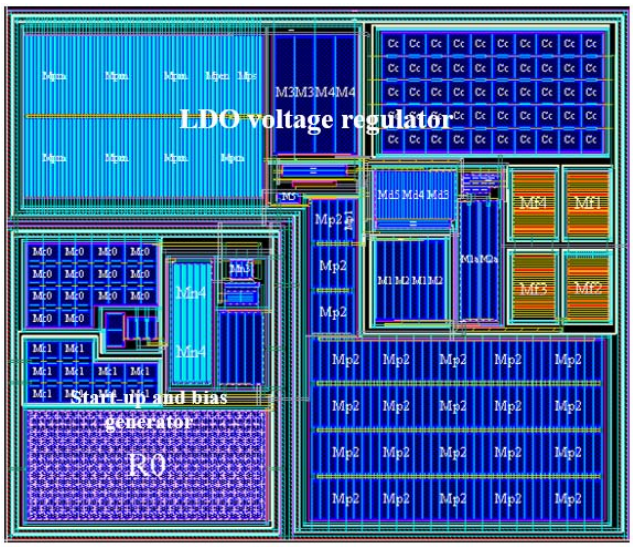

Figure 15. Integrated LDO Chip Layout

Fig. 15 is the integrated startup, bias generator and LDO chip layout with area of 160.1µm x 180.2µm. Transistors in the LDO circuit are layout in common centroid for proper matching. Shortest possible route and alternating of metals are one of the techniques used to avoid large parasitic capacitance and parasitic resistance.

TABLE 3. Comparison on previous works

Parameters	This Work	Chong, S., et.al.	Zhang, B., et.al.	Guo, J., et.al.
Technology	65 nm	65 nm	130 nm	90 nm
Input voltage (V)	0.8 ~ 1.2	1 ~ 1.2	1 ~ 1.2	0.75 ~ 1.2
Load Current	0 ~ 100 mA	0 ~ 100 mA	1uA ~ 100 mA	0 ~ 100 mA
Dropout Voltage	135 mV	200mV	200mV	250mV
Output voltage (V)	0.6	1	0.8	0.5
$C_{comp.}$ (pF)	3.5	4.5	2.5 & 0.8	7
C_{load} (pF)	0 ~ 100	0 ~ 100	100	0 ~ 50
ΔV_{out} (mV)	86	68.8	50	114
ΔI_{load} (mA)	100	100	10	97
Line Regulation	0.158 mV/V	4.7 mV/V	3.5 mV/V	3.78 mV/V
Load Regulation	0.158 mV/mA	0.3 mV/mA	0.14 mV/mA	0.1 mV/mA
PSRR (dB)	-63.20 (10 kHz)	-58 (10 kHz)	-36 (1MHz)	-44 (10 kHz)
Quiescent Current	930.21 nA	900 nA	2.9 uA	8 µA
Area	160.1µm x 180.2µm	-	-	-

IV. CONCLUSION

A low-voltage, ultra-low quiescent current output-capacitor-free LDO voltage regulator proposed and implemented in 65nm CMOS process using Synopsys Tool. With the system working at 800mV supply voltage, subthreshold operation and power transistors in saturation, an ultra-low power consumption at no-load is achieved at 744.17nW with high current efficiency in light and heavy loads. A regulated output of 600mV with good stability and transient responses for the entire load current range of 1pA to 100mA with the use of the adaptive multi-gain stage structure. In comparison with prior works of art, the designed LDO voltage regulator has lower quiescent current, better stability margins, and good performance in load, line regulation, voltage variation, and PSRR. The researcher recommends further studies on the use of a temperature-independent current reference and increase in the stability of the error amplifier.

ACKNOWLEDGMENT

The author would like to commend and give gratitude to Department of Science and Technology - Engineering Research and Technology for Development (DOST-ERDT), for funding and sponsorship and Analog Devices, Inc. – Philippines (ADGT) being the mentor of this study.

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